Experimental Evaluations for the Relationship between Program Performance and Lifetime of NAND Flash Memory

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Abstract

The Nand based storage products are emerging as a main storage of portable systems such as notebook or mobile systems. In embedded devices including mobile systems, much faster program performance and longer lifetimes are becoming more important. The lifetime and performance have trade-off relationship as is well known. But there are no previous studies which explicitly show the relationship experimentally. We measured the variation of lifetime and performance both in accordance with the program voltage changing rather than focusing only on either side. We also carried out additional experiments to find the maximum program/erase cycles limitation that does not lead to lifetime's loss but can have gains of program performance. Our experimental results can be utilized in various software layers. They also can contribute to software design which takes full advantage of lifetime and performance characteristics of Nand flash memory.

1. Introduction

Nand flash memory (hereafter Nand) was employed as the secondary data storage in the past. But it has sharply emerged as a main storage of the system since 2000. Notably, Nand became universal and general data storage with the development of Nand based solution products such as Multi Chip Packages(MCPs) and Embedded Multimedia Cards(eMMCs). Especially, Solid State Disk(SSD) is spotlighting as a main storage of notebook or desktop, substituting Hard Disk Drive (HDD) in recent years.

Therefore in-depth understandings on the behaviors and the natures of Nand, particularly performance and lifetime, are becoming increasingly important. There are many device physics researches associated with reliability characteristics of Nand transistor level[1,2,3]. Some studies were interested in endurance of Nand solution products or systems based on it[4,5,6]. A little studies for improving either performance or lifetime have been actively carried out[7,8]. Performance and lifetime have trade-off relationship. However, the majority of studies have focused on either lifetime or performance. There were no previous studies which investigated experimentally and comprehensively for the trade-off relationship as far as we know.

In this paper, we investigate program time(tPROG) and endurance changes according to the program start voltage(Vstart) and program stepping voltage(Δ ISPP). They are elements of Incremental Step Pulse Program scheme(ISPP)[9]. We will also discuss the utilizations of the experimental results on various software layers such as firmware and file systems.

2. Nand Flash Program Operation

Incremental Step Pulse Program (ISPP) is the bit-by-bit Program and Verify algorithm[9] for adjusting threshold voltage(Vth) of programmed Nand cell. The algorithm is as follows: Firstly, program with "Vstart" in all targeted cells and check the Vth of programmed cells by read operation called "Verify". Secondly, inhibit programmed cells which have higher Vth than specific verify level(Vvfy). Thirdly, reprogram the rest of cells with much higher Vpgm elevated as Δ ISPP. Finally, the program operation will be terminated when the Vth of all cells are over targeted Vvfy. Verify level is always constant to Vvfy in this algorithm.

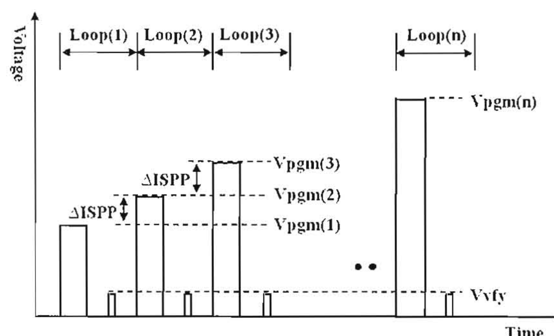

Figure 1. Incremental Step Pulse Program(ISPP) scheme during program operation

Vpgm(1) is initial start Vpgm level, Vstart, Vpgm(2) which is the next reprogramming start voltage, is set to

Δ ISPP + Vpgm(1). Final reprogramming start voltage can be expressed as follows.

$$Vpgm(n)=Vpgm(1)+(n-1)\Delta ISPP \quad (1)$$

The internal program time(tPROG) can be reduced as decreasing the number of program loop(Loop(n)). Much higher Vpgm by increasing the program loop count "n" adversely affect reliability characteristic of Nand. It is the acceleration of oxide degradation.

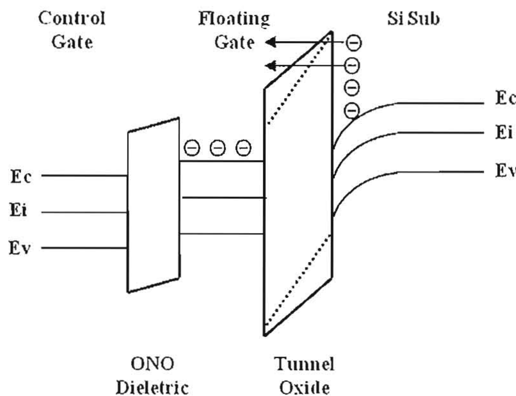

Figure 2. Schematic energy band bending diagram when program operation

Schematic energy band bending diagram during program operation is shown in Figure 2. Strong energy band bending takes place downwards from surface area of Si-sub when positive voltage is applied to the gate. Thereby electrons are gathered in surface area of Si-sub. From the perspective of electrons, Energy barrier width getting smaller, the FN tunneling takes place consequently [10]. The amount of electrons that pass through the tunnel oxide during FN tunneling are the function of the electric field[11]. Much higher voltage induces much larger electric field. Thereby electrons injection amount to floating gate are increased. If we make Vpgm(1) or Δ ISPP in Figure 1 much larger, much higher Vpgm will be applied on the gate. Much strong electric field formed across the tunnel oxide leads to even smaller energy barrier width of oxide (Figure 2, dashed line). So, FN tunneling will occur more easily. It implies that we have to apply strong voltages as high as available on the gate for program performance gains. However, the oxide degradation (one of the major reliability issues in Nand) is closely related with those voltages. Fast/slow interface trap [Nit] and Oxide trap[Not] are generated during P/E cycles by FN current stress. They make the tunnel oxide[1,2,3] to degrade and there are several electron trap mechanism: electron injection, hole injection into oxide, electron trap generation, etc[3]. The amount of electrons trapped in oxide during P/E cycles are the form of a power-law[1]. The higher Vpgm lead to the larger FN current stress and it accelerates the oxide degradation. Consequently, endurance failure arises much more quickly. Here, endurance failure does not mean permanent damage of tunnel oxide that no more FN tunneling is available. It means transient read failure by widen distribution or by Vth shift of cells caused by increment of the trapped electrons. Many studies discussing the cure effects of degraded oxide support above descriptions[1,2,3].

More details relevant to Nand flash memory are well shown in [11].

3. Experimental Results

3.1 Methodology

We tested 5 MLC Nand chips that are manufactured by the latest process. All evaluations were done at room temperature(25'C). We hired endurance as an indicator of lifetime. We regard the point of endurance failure in the same light as the end of lifetime. We carried out read operations periodically during P/E cycles. Read failure occurrence imply that the amount of failure bits exceed the Error Correction Code (ECC)[12] tolerance level (72bit/2Kbyte, appeared in Nand datasheet[13]). We identified the point of read failure arising with endurance failure point. We programmed with different data patterns during each P/E cycle to create four MLC data states evenly on all cells. Evaluation size of each condition was 8 blocks(1024pages). We hired tPROG appeared in Nand flash datasheet[13] as an indicator of program performance. The tPROG measurement sizes for each condition were 2 blocks(256pages).

3.2 Program Performance vs. Lifetime

We carried out our experimentation on program operation using 4 differentiated data patterns to inflict even stresses on every physical cell while measuring endurances. We conducted single read operation on every 500 times P/E cycles. There were no pause times during P/E cycles. Our test sizes for each condition were 40ea Nand blocks(8blocks/chip x 5chips). We calculated representative endurance in the manner of averaging all endurances of test blocks.

Figure 3 shows the tPROG and endurance results according to the initial program start voltage, Vstart, changes. "Default" means initial value set in memory chip. We can recognize that the measurement results are getting smaller as Vstart levels increasing. It

signifies faster program time and reduced lifetime. We discovered special and beneficial regions by the experiment of reducing Vstart levels: default-0.1V ~ default-0.4V. The results of those ranges show that a little endurance increment(up to 4.5%) can achieve as nearly same program speed as "default". Maximum performance gains due to the increment of Vstart level was up to 20%.

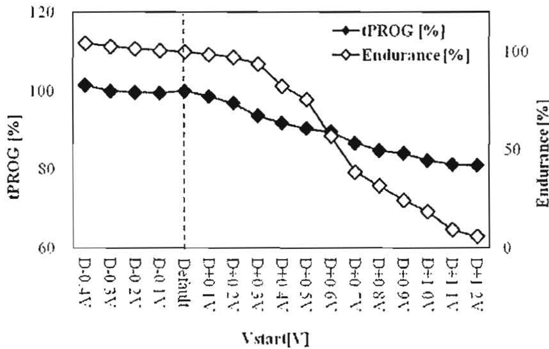

Figure 3. Program performance vs. lifetime as variation of Vstart

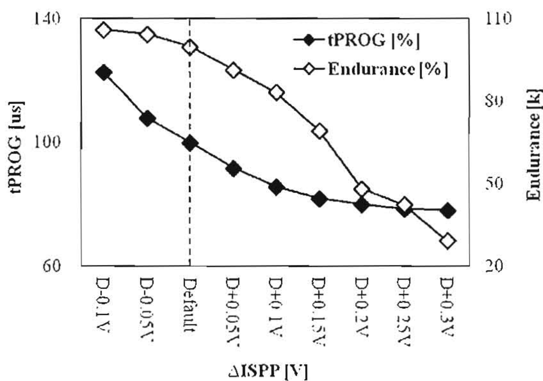

Figure 4. Program performance vs. lifetime as variation of Δ ISPP

In case of Δ ISPP changing as shown in Figure 4, we were able to confirm the trade-off relationship of program performance and endurance for all measured ranges. Maximum performance gains was up to 22% when Δ ISPP grown up and lifetime gains was up to 6% with lowered Δ ISPP, respectively.

We could get up to 22% program performance gains when applying higher Vpgm than default as shown in Figure 3 and 4. This result can be utilized in diverse functions of firmware side that fast program speed is preferred: sequential write, Nand block swapping such as garbage collection and wear-leveling. Meanwhile, lower Vpgm corner cases are able to get lifetime gains up to 6%. They also can be exploited in case that data reliability is more important such as metadata write of file system or firmware. The endurance and program performance have the trade-off relationship. Because of this, software designer should consider the loss of the other side against gains of one. For instance, endurance characteristics should be degraded if Vstart or Δ ISPP levels are increased for fast merge operation. In this case, it is mandatory to manage erase count, considering the endurance degradation.

3.3 Additional Experiments

We did trying to find the maximum P/E cycles which not lead to lifetime loss almost or at all but can have performance gains by additional experiments. The additional experiments have different methodologies from experiments of Section 3.2. It used upward Vpgm for performance gains and reverting elevated Vpgm to default after specific number of P/E cycles. Additional experiments were begun under the assumption that the endurance failure will not arise by the only one time programming with elevated Vpgm level on target cell. Our experiments were carried out on the three elevated Vpgm corners which can have program performance gains up to 10~22%.

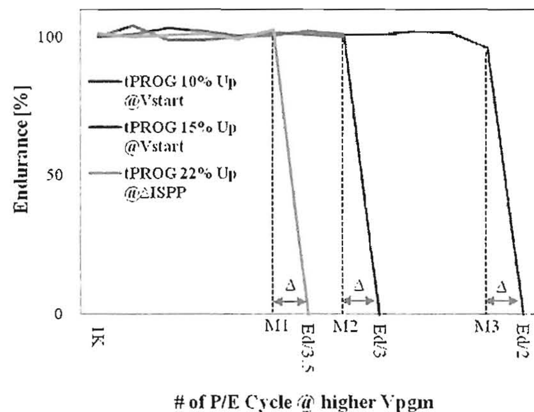

Figure 5. Endurance at combination of higher Vpgm and default Vpgm

The experiments were carried out in the manner of comparing default endurance("Ed") with enduracne ("Mn+Kn") obtained from the combination of two different Vpgm levels(elevated and default Vpgm). Firstly, P/E cycles are conducted to "Mn"(here n=1~3) times with each elevated Vpgm. Secondly, changing Vpgm to default and execute extra "Kn"(here n=1~3)

times of P/E cycles. Lastly, new endurance can be calculated by "Mn+Kn". We employed trial and error approaches to find "Mn" and learned that "Mn+Kn" is almost close to "Ed". It has been observed that higher Vpgms for program performance gains did not almost affect the entire lifetime until the particular P/E cycle numbers "Mn". The x-axis of Figure 5 shows "Mn", P/E cycle number executed by higher Vpgm. "Ed"/3.5, "Ed"/3, "Ed"/2 which appeared in x-axis are decreased endurance failure points corresponding elevated Vpgm which can get performance gains up to 22%, 15%, 10%, respectively. The y-axis is the ratio of new endurance "Mn+K" against "Ed". According to the experimental results, new endurance and default endurance did not differ until "Mn" reaches to decreased endurance failure point - Δ for all three corner conditions. Here, Δ is approximately 500 times. It is a quite surprising result considering that our additional experiments took place in room temperature and P/E cycles are carried out continuously without pause time until endurance failure. It is considered to be difficult to expect charge detrap effects[1,2,3,6]. We argue that it opens new opportunities in software layers such as firmware and file systems: for instance, mixed voltage programming mechanism controlled by the software layers can be used to increase program performance without degrading endurance.

4. Conclusion

The most major constraint for gaining program performance is corresponding lifetime loss in Nand. In this study, we investigated experimentally the trade-off relationship between performance and lifetime in raw Nand manufactured by the latest process. We measured endurance and tPROG as the indicators of lifetime and performance, respectively, by changing two elements of ISPP (Vstart, Δ ISPP). To ensure the accuracy of our experiments, we occupied differentiated I/O patterns which are making uniformly 4 data states of MLC to all tested cell during P/E cycles. We could have tPROG gains up to 22% and endurance increment up to 6% according to the experimental results. We learned that lifetime loss did not arise even if we conduct program with the elevated Vpgm until slightly ahead of original decreased endurance failure point corresponded to that elevated Vpgm. Our experimental results can be used in various software layers and diverse functions that faster program performances or longer endurances are preferred. By the benefit of our experimental results, system designs to take full advantage of Nand property can be made and the flexibility of software design can be improved.

5. Future Work

We are planning to design software systems which can exploit our experimental results. We will evaluate the lifetime and performance variation with diverse functions on the system. The results of our additional experiments gave many questions and inspirations to us and they may need further progress. We are also a lot interested to erase operation. Erase has the same mechanism (FN tunneling) with program. Erase may lead even more impact to Nand based storage systems caused by longer internal execution time than program. We are planning to investigate the relationship of the performance and lifetime for erase operations in the same way as program operation of this study.

6. Acknowledgement

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